

IEEE Workshop on Representations of PEGD Studies



FPGA-based simulations for power electronics and power systems applications

5th December 2019



OPAL-RT
TECHNOLOGIES

1. **OPAL-RT TECHNOLOGIES**
2. CONTEXT & CHALLENGES
3. FPGA-BASED SOLUTIONS
4. APPLICATION CASES
 - MOTOR DRIVES
 - DISTRIBUTION GRIDS
 - TRANSMISSION GRIDS (HVDC)

OPAL-RT TECHNOLOGIES

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OPAL-RT
TECHNOLOGIES

OPAL-RT manufactures high-end **real-time simulators**, scaling from compact portable devices to integrated HIL test benches. OPAL-RT systems are deployed for *design, validation and optimization* of complex control systems through **Control Prototyping** and **Hardware in-the-loop** approaches.



 **OPAL-RT**
TECHNOLOGIES

FIGURES

OPAL-RT Technologies Inc.

- Created in 1997
- 230 employees (25 nationalities)
- Headquarters in Montreal, Canada
- 5 local subsidiaries
- A network of 20+ distributors



900 customers worldwide



OFFICES & SECTORS

5



ELECTRICAL



AUTOMOTIVE



AEROSPACE
& DEFENCE



OTHER INDUSTRIES



ACADEMIC
& RESEARCH



OPAL-RT
TECHNOLOGIES

AGENDA

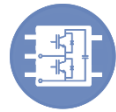
1. OPAL-RT TECHNOLOGIES
- 2. CHALLENGES**
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COMPLEX SYSTEMS – CHALLENGES

7



Very **complex** and sophisticated systems



New technologies for electrical systems



More **complex** control and protection strategies



New IT approaches

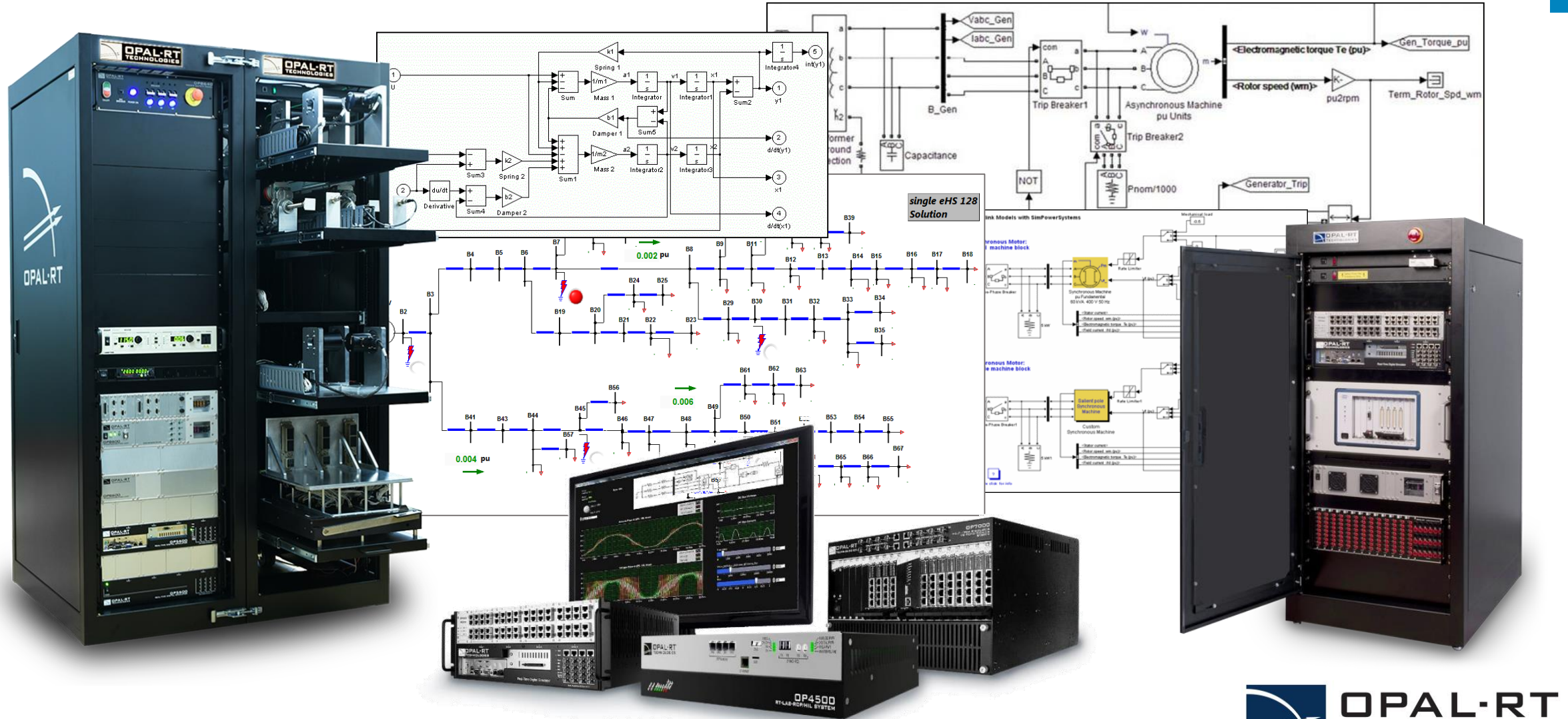


On-field tests **hard** to conduct



COMPLEX SYSTEMS – CHALLENGES

8



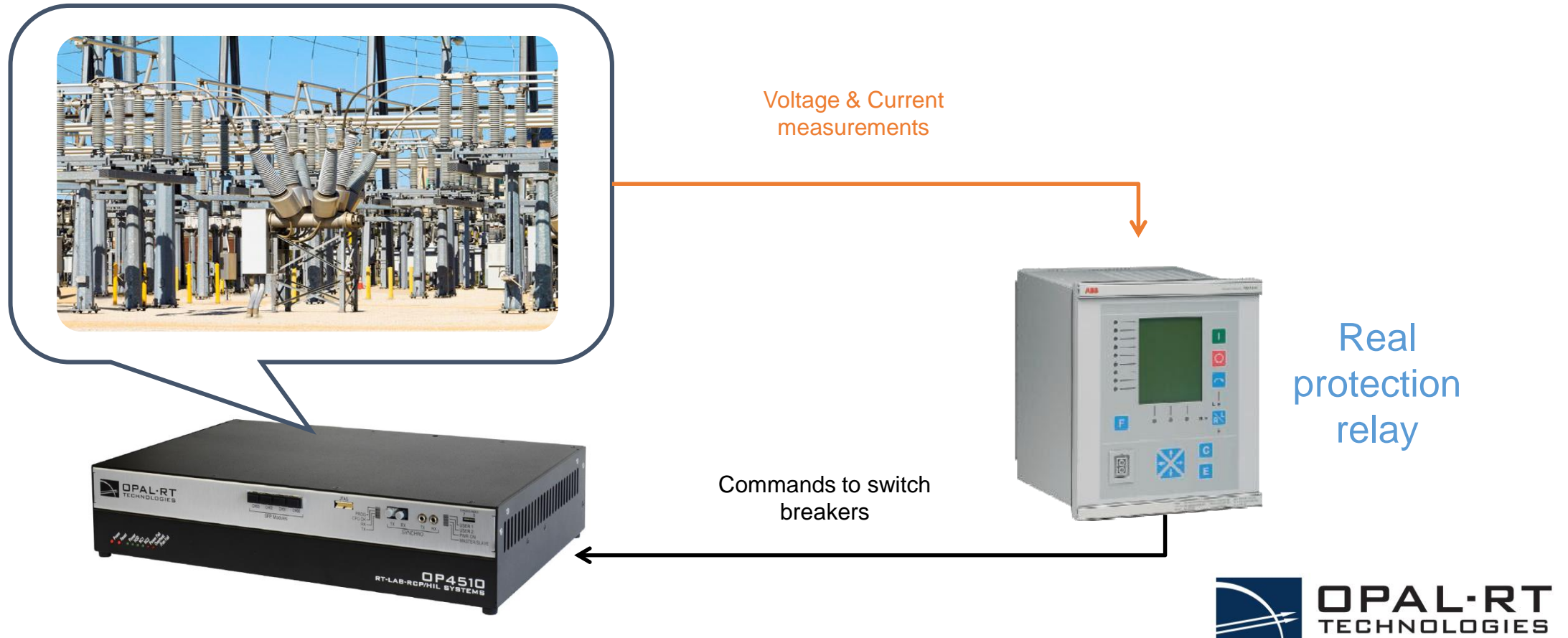
A MODEL ? WHAT FOR ?

- Facilitate the development of complex control systems
- Use less physical prototypes
- Test complex/dangerous cases is a safe way
- Replace missing hardware by software models

COMPLEX SYSTEMS – CHALLENGES

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TO TEST A CONTROL OR PROTECTION DEVICE IN A GRID... **WITHOUT A GRID !**

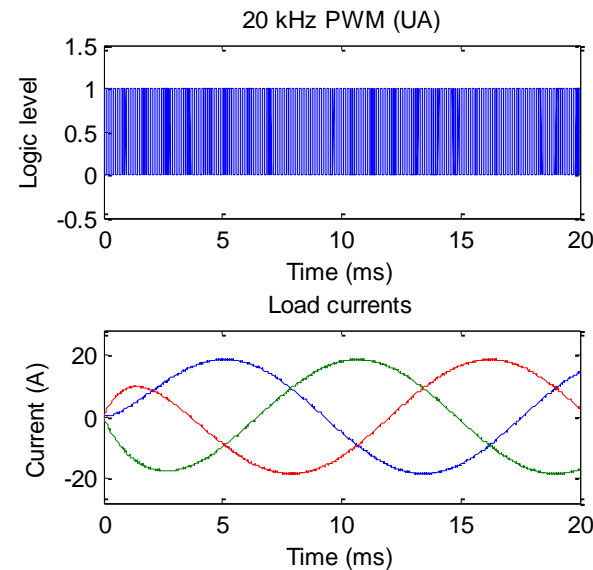
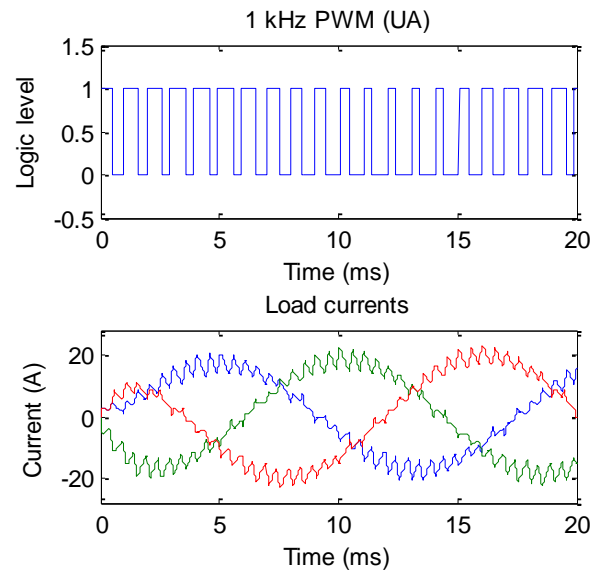


- Simulation of more **complex** electrical circuits
- Need for more **representative/accurate** models
- Need to sample signals very **precisely**
- **Higher switching** frequencies for power electronics (SiC, GaN)

COMPLEX SYSTEMS – CHALLENGES - FOCUS ON ACCURACY

12

- Higher switching frequencies (>100 kHz) – *SiC*, *GaN*
- Higher power density, lower THD
- Requires higher sampling rates ($< 1 \mu\text{s}$)

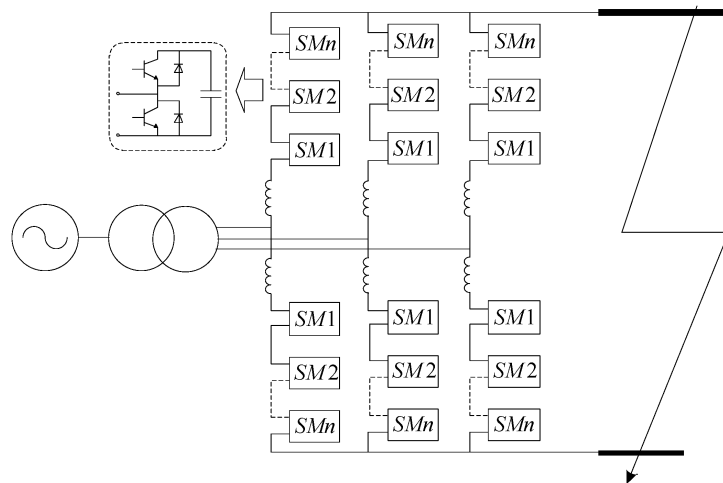


COMPLEX SYSTEMS – CHALLENGES FOCUS ON COMPLEXITY

13

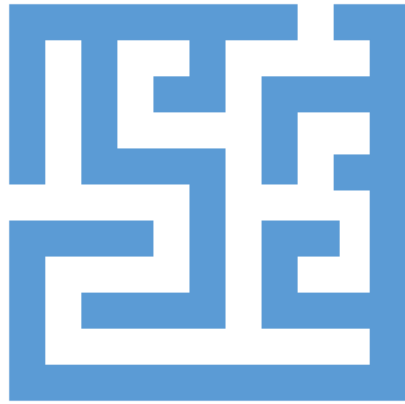
Modular Multilevel Converters for HVDC

- N submodules (SM) per arm (N -> 500)
 - Up to 5 switches per SM
- Up to **15 000 switches** per converter



COMPLEX SYSTEMS – CHALLENGES

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Complexity



Accuracy



Speed

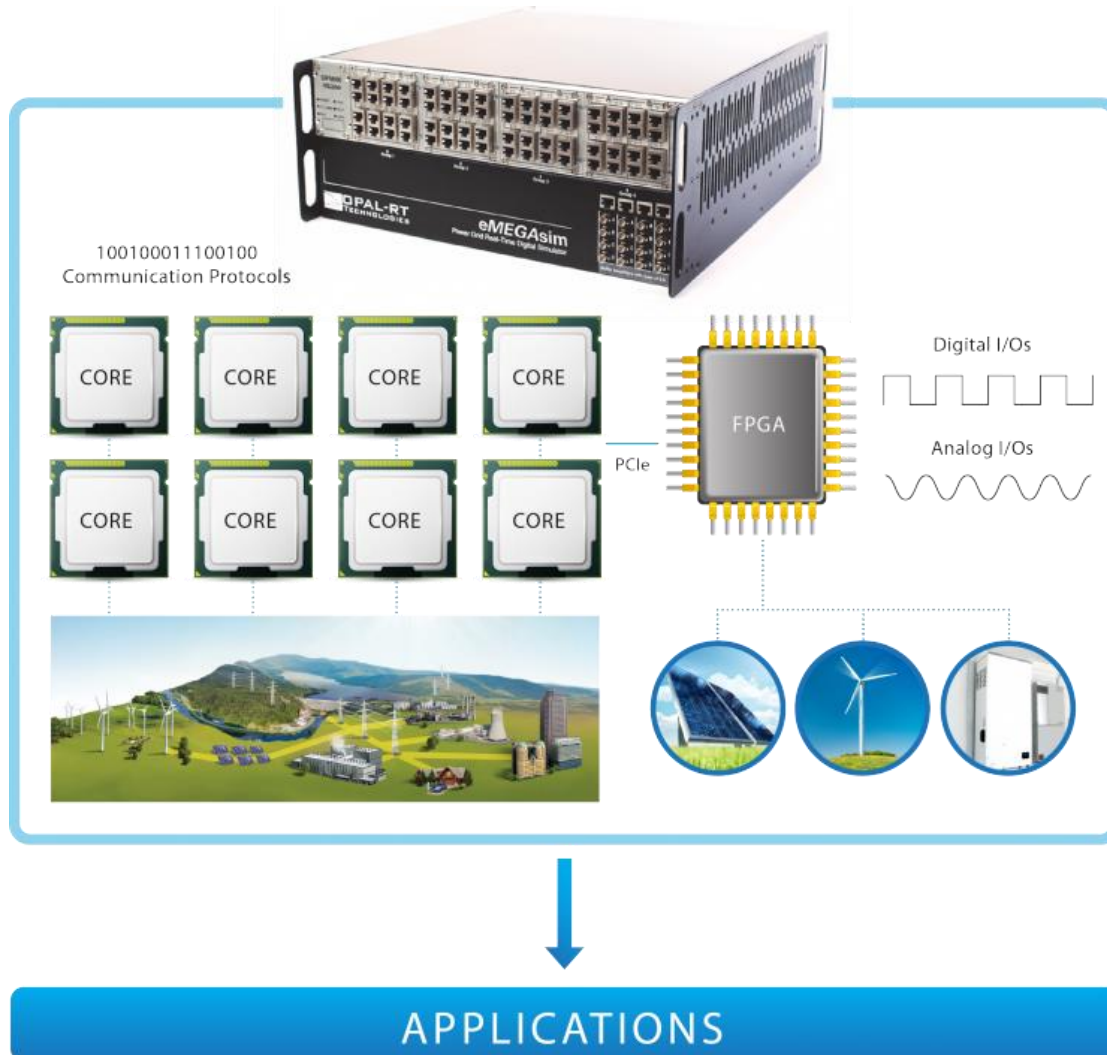
1. OPAL-RT TECHNOLOGIES
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CPU & FPGA CO-SIMULATION

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All OPAL-RT systems take advantage of both CPU and FPGA resources.

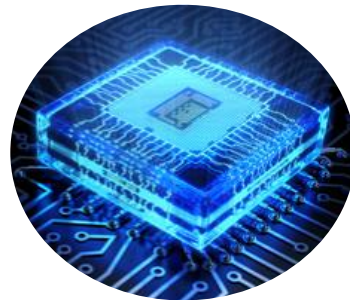
- **CPU:** massive computation power
 $T_s > 10 \mu s$
- **FPGA:** great accuracy and low latency
 $T_s < 1 \mu s$



ONE SOLUTION: FPGA SIMULATION

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- **ACCURATE:** Low sampling time and therefore excellent resolution for high frequency switching (up to 50-100 kHz)
- **FAST:** Excellent execution latency (typ. 1 μ s)
- **PARALLEL:** Massively parallel processing unit



- **COMPLEX DESIGN:** Higher coding complexity ('for' loop, division, ...)
- **TIME CONSUMING:** Very long compilation time (~hours)
- **DIFFICULT DEBUGGING:** Increased debugging difficulty

$$\begin{aligned}
 \frac{dV_1}{dt} &= \frac{1}{C_1 R} (V_2 - V_1) - \frac{g(V_1)}{C_1} \\
 \frac{dV_2}{dt} &= \frac{1}{C_2 R} (V_1 - V_2) - \frac{I_L}{C_2} \\
 \frac{dI_L}{dt} &= -\frac{V_2}{L}
 \end{aligned}$$

$$\begin{aligned}
 a \frac{d^2 y}{dt^2} + a_1 \frac{dy}{dt} + a_2 y &= G(t) \\
 a y'' + a_1 y' + a_2 y &= G(t)
 \end{aligned}$$

$$\begin{aligned}
 I_a - C_1 \frac{de_1}{dt} - \frac{1}{L_2} \int (e_1 - e_2) dt - \frac{e_1}{R_1} - \frac{1}{L_1} \int e_1 dt &= 0 \\
 C_1 \frac{de_1}{dt} + \frac{e_1}{R_1} + \left(\frac{1}{L_2} + \frac{1}{L_1} \right) \int e_1 dt - \frac{1}{L_2} \int e_2 dt &= I_a \\
 \text{differentiate to get rid of integrals} \\
 C_1 \frac{d^2 e_1}{dt^2} + \frac{1}{R_1} \frac{de_1}{dt} + \left(\frac{1}{L_2} + \frac{1}{L_1} \right) e_1 - \frac{1}{L_2} e_2 &= I_a \\
 C_1 \ddot{e}_1 + \frac{1}{R_1} \dot{e}_1 + \left(\frac{1}{L_2} + \frac{1}{L_1} \right) e_1 - \frac{1}{L_2} e_2 &= I_a
 \end{aligned}$$

$$\begin{aligned}
 N_1^w &= \frac{\beta_1^r l^2 \xi (\xi^2 - 3) - 24 \beta_2^r \xi}{4 \beta_1^r l^2 + 48 \beta_2^r} + \frac{1}{2}, \quad N_2^w = \left[\frac{l}{8 \beta_1^r} - \frac{l^3 \xi}{8 \beta_1^r l^2 + 96 \beta_2^r} \right] (1 - \xi^2), \quad N_3^w = \beta_3^r \left[\frac{l}{8 \beta_1^r} - \frac{l^3 \xi}{8 \beta_1^r l^2 + 96 \beta_2^r} \right] \\
 N_4^w &= \frac{\beta_1^r l^2 \xi (3 - \xi^2) + 24 \beta_2^r \xi}{4 \beta_1^r l^2 + 48 \beta_2^r} + \frac{1}{2}, \quad N_5^w = \left[\frac{l}{8 \beta_1^r} + \frac{l^3 \xi}{8 \beta_1^r l^2 + 96 \beta_2^r} \right] (\xi^2 - 1), \quad N_6^w = \beta_3^r \left[\frac{l}{8 \beta_1^r} + \frac{l^3 \xi}{8 \beta_1^r l^2 + 96 \beta_2^r} \right] (\xi^2 - 1)
 \end{aligned}$$

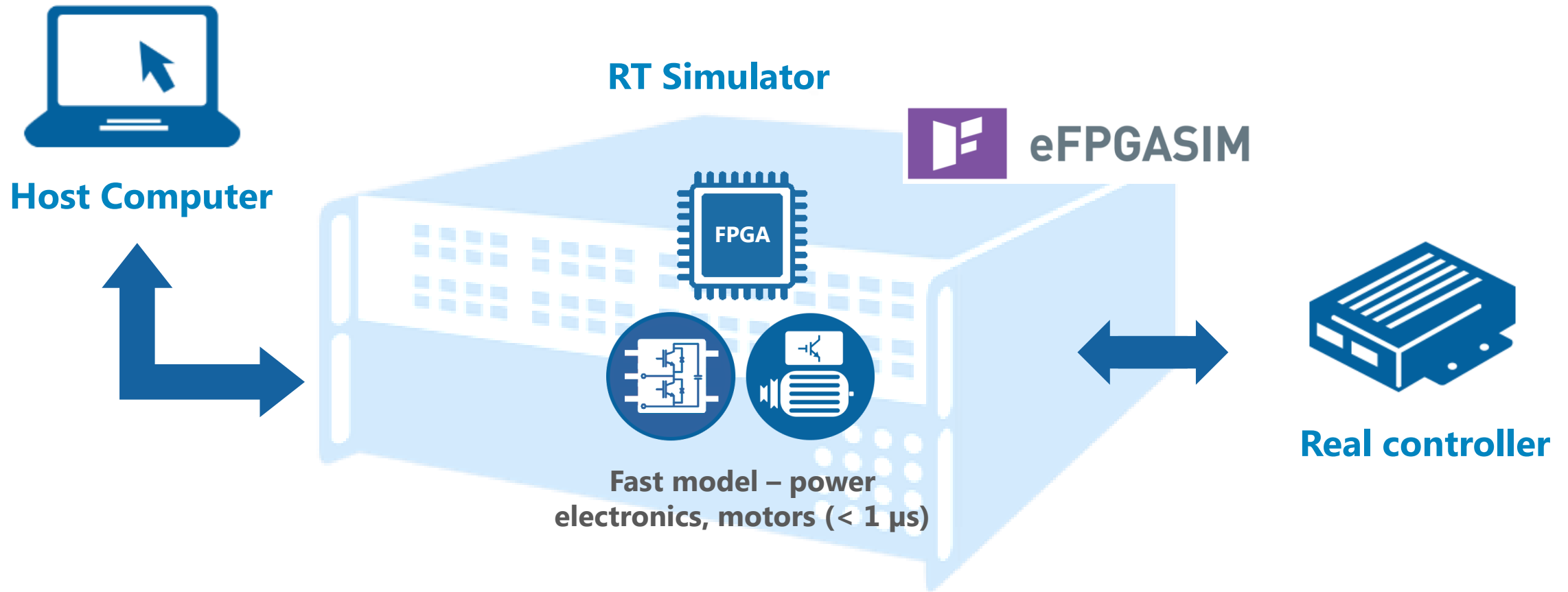


eFPGASIM

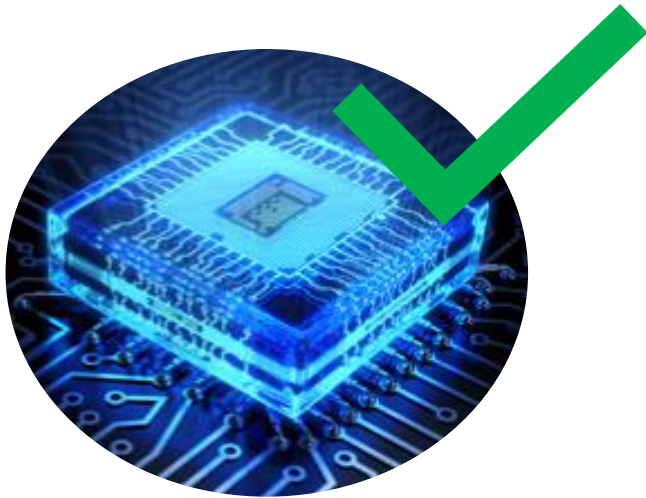
Set of **models** and **solvers** designed to facilitate the fast and accurate simulation of **electrical circuits on FPGA**, as well as associated services *(gating signals, sensor emulation, communications)*

MOTOR DRIVES – eHS CONCEPT

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FPGA performance

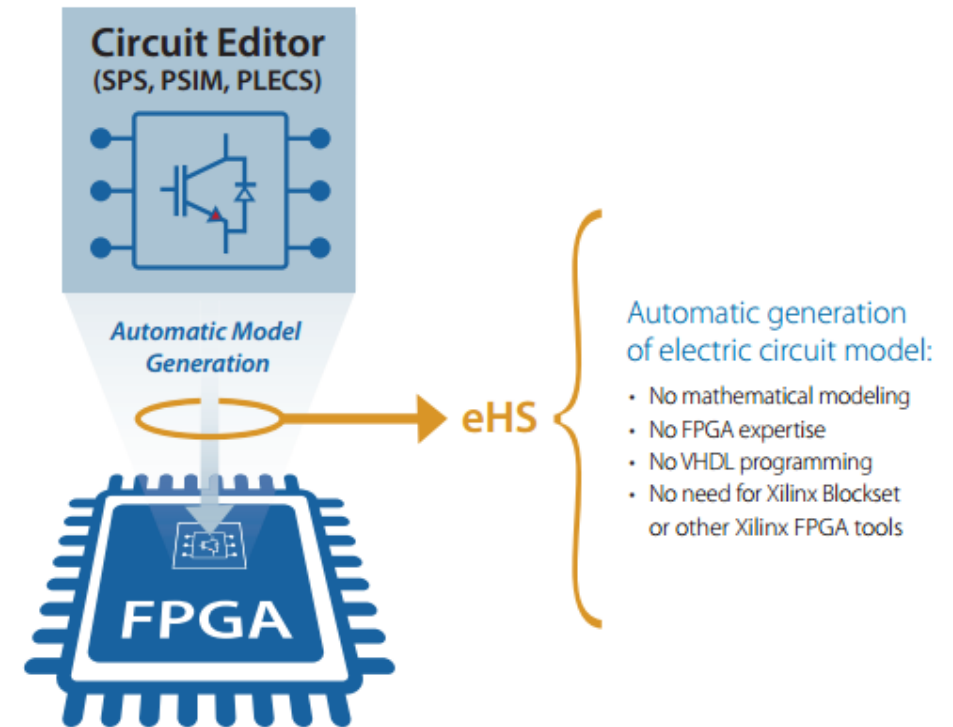


FPGA ease of use



eHS: **e**lectrical **H**ardware **S**olver

- Allows the use of a **comprehensive circuit editor** ...
- ... while taking advantage of the **FPGA performance** ...
- ... **without writing** a single line of HDL code !



MOTOR DRIVES – eHS CONCEPT

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Model Name: Untitled4 [v0.3.0]

HOME VIEW

File Edit Clipboard Drawing Format

PALETTE MODEL BROWSER

SYSTEM

- Import
- Output
- Electrical Node
- Ground
- Power Port
- Subsystem

This block provide an output port for a subsystem or model.

arm3

This component implements a 3-level DC to AC ne converter. It enable

Gate Mapping

SOURCE

1	NC
2	NC
3	NC
4	NC

Parameters

Forward voltage (V)

Switch ad

Internal re (Ron)

Initial con (s)

Cancel

V_{in}

SOURCES

☒ SIMULINK

AI A1 = V_{in}

Pin A1

Gain 1 V/V

Offset 0 V

Min -Infinity V

Max Infinity V

PICK YOUR SIMULATOR

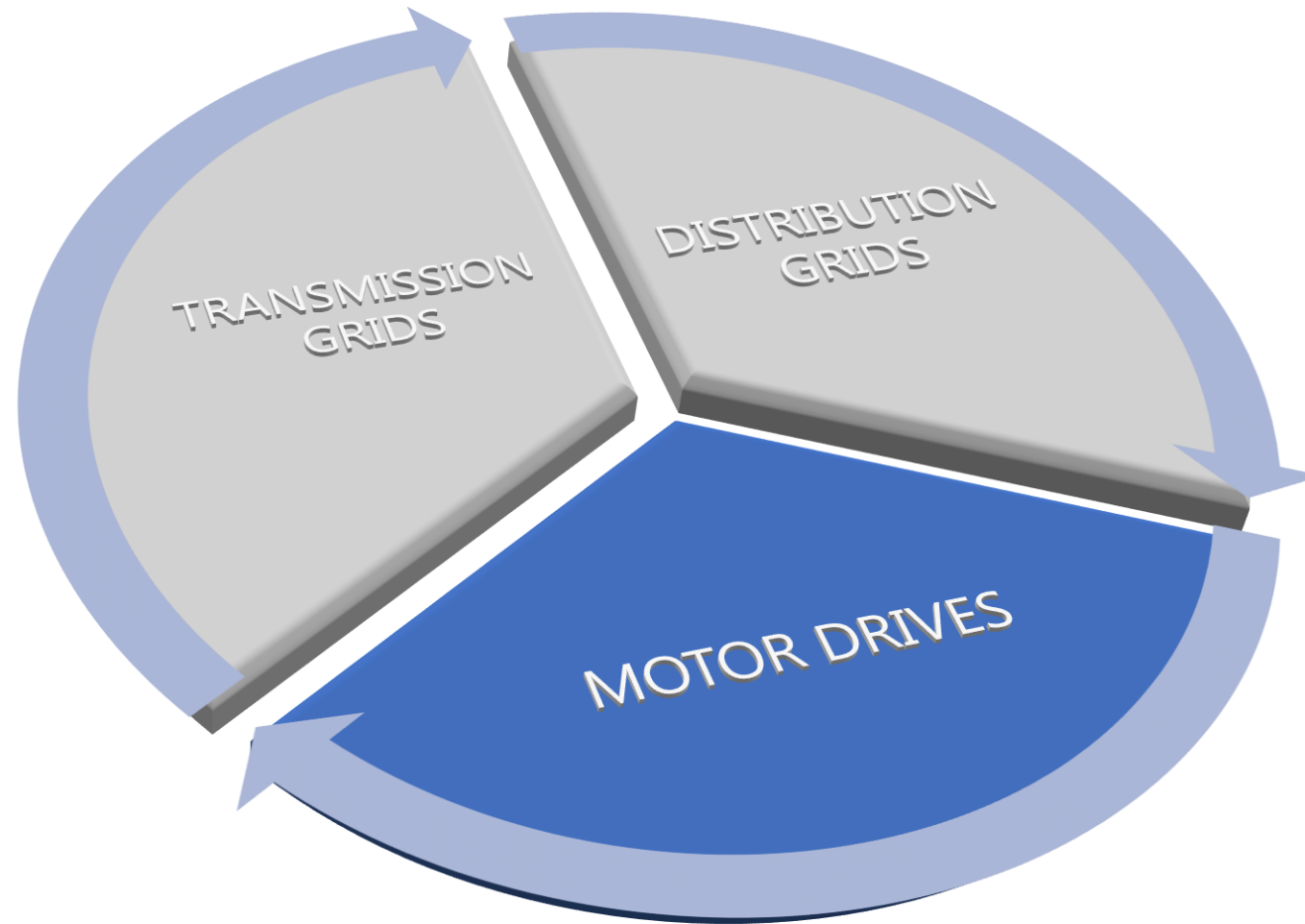
- Local
- OP4200
- OP4510
- OP5707

The screenshot displays the eHS Concept software interface. The main workspace shows a circuit diagram of a 3-level DC to AC converter. The circuit includes a DC source, a split DC link with two capacitors, three inverter legs, and a three-phase motor load. One inverter leg is highlighted with a blue box. On the left, a 'SYSTEM' palette lists components like 'Import', 'Output', 'Electrical Node', 'Ground', 'Power Port', and 'Subsystem'. A tooltip for the 'Output' block states: 'This block provide an output port for a subsystem or model.' On the right, the 'PROPERTIES SIDE' panel shows settings for the 'arm3' component, including a 'Gate Mapping' table and 'Parameters' for forward voltage, switch, internal resistance, and initial condition. Overlaid on the right is a 'V_{in}' dialog box with a 'SOURCES' tab where 'SIMULINK' is selected, and a 'PICK YOUR SIMULATOR' dialog box with options for 'Local', 'OP4200', 'OP4510', and 'OP5707'.

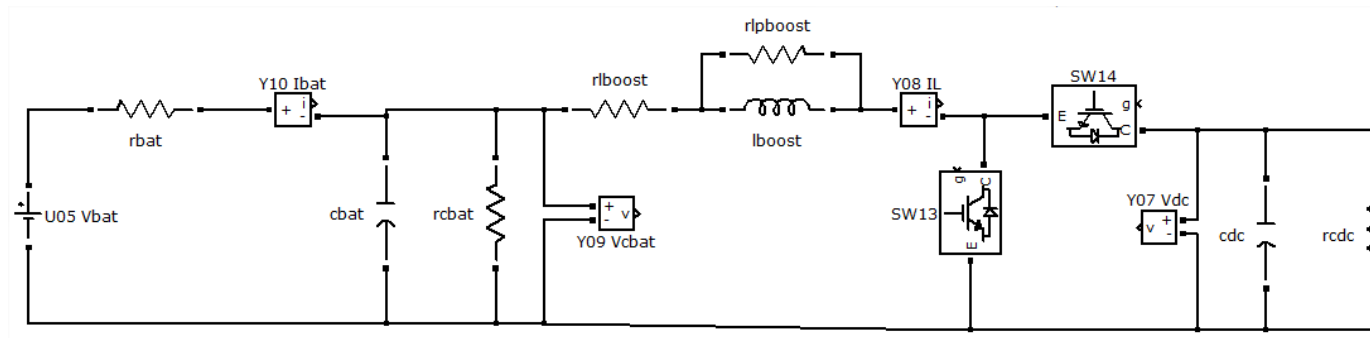
AGENDA

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 - **MOTOR DRIVES**
 - **DISTRIBUTION GRIDS**
 - **TRANSMISSION GRIDS (HVDC)**

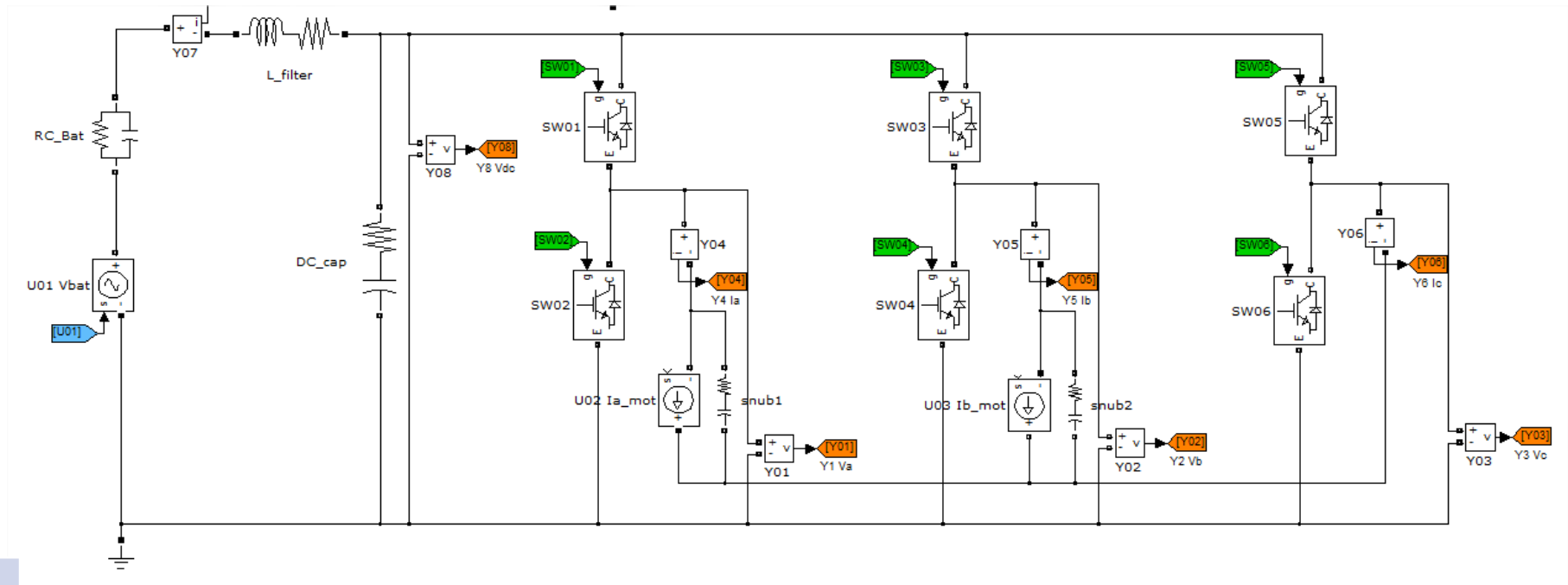
APPLICATION CASES



INITIALLY...

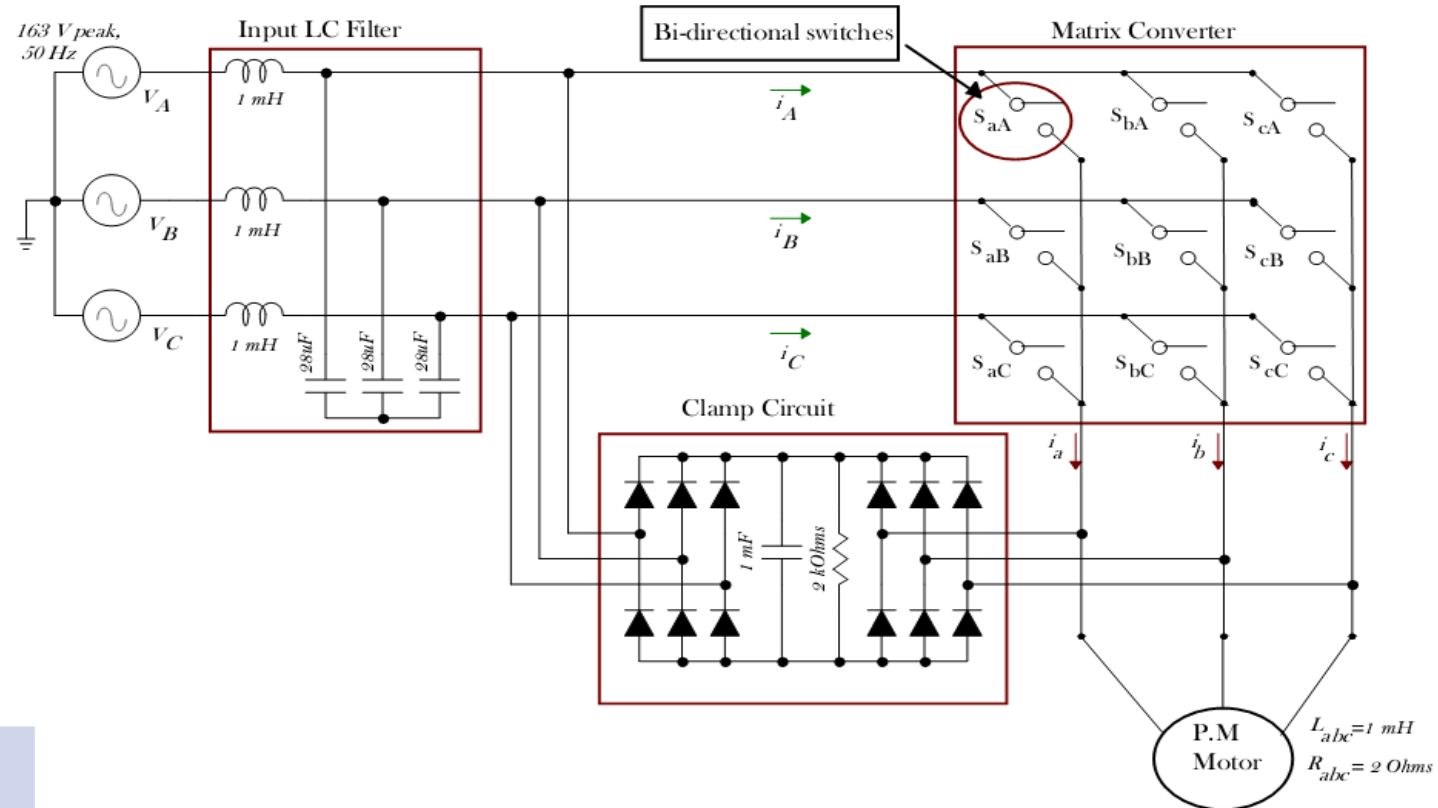


Boost
Model Time Step = **150 ns**
10 kHz PWM



3-phase 2-level Inverter
Model Time Step = **200ns**
50 kHz PWM

States	5
Switches	6
Inputs	4
Outputs	8



States

7

Switches

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Inputs

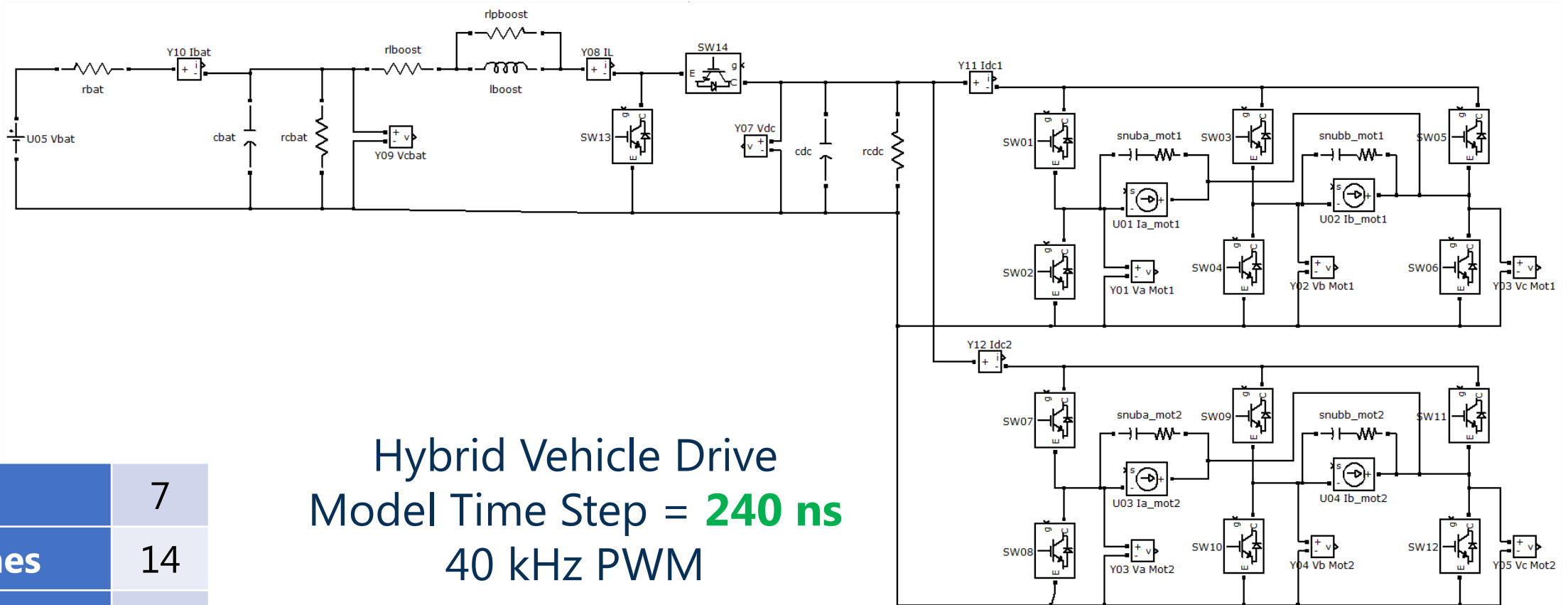
3

Outputs

8

Matrix converter drive
Model Time Step = **350 ns**

MOTOR DRIVES

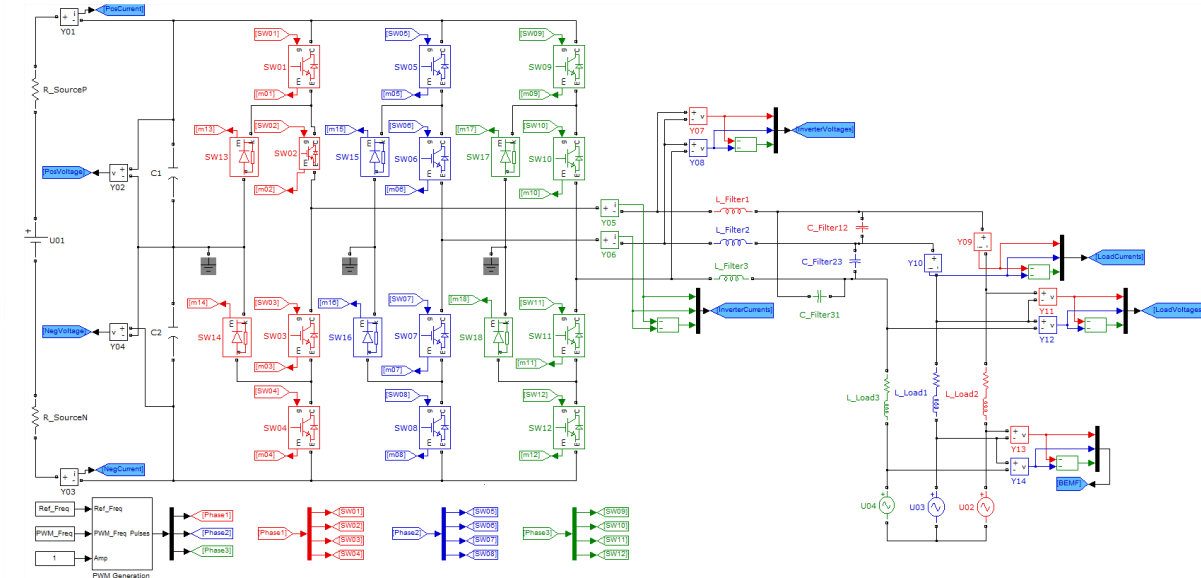
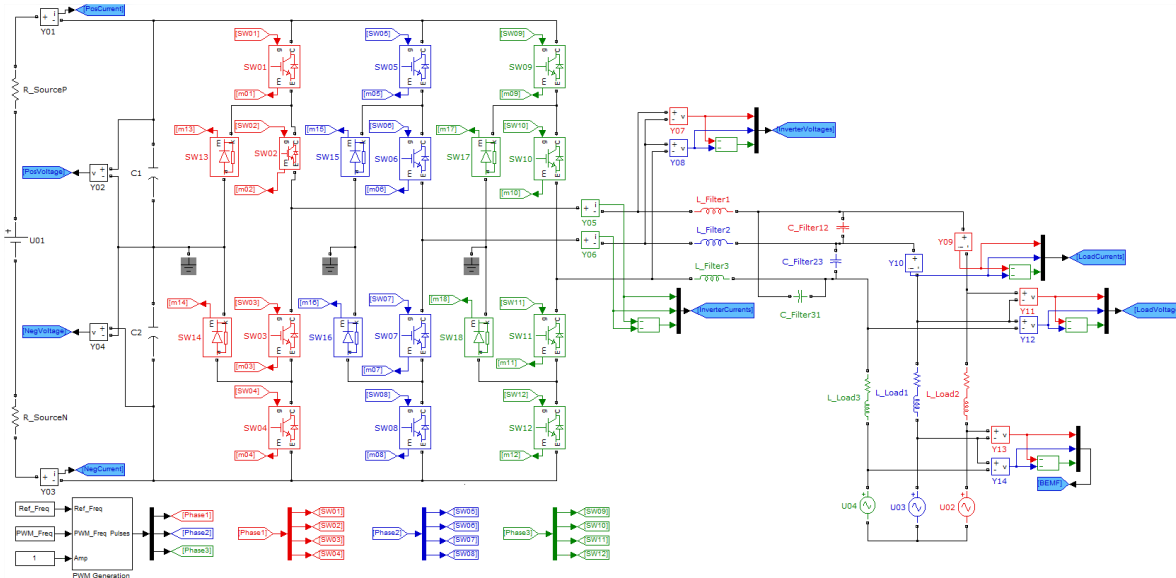


Hybrid Vehicle Drive
Model Time Step = **240 ns**
40 kHz PWM

States	7
Switches	14
Inputs	5
Outputs	12

MOTOR DRIVES

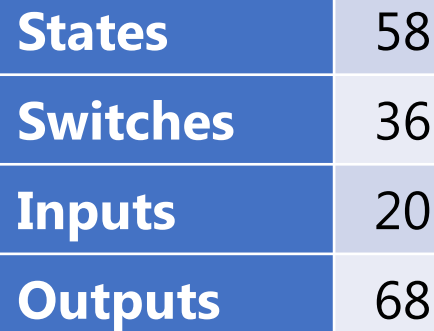
30



States	22
Switches	36
Inputs	8
Outputs	28

2 x NPC 3-phase 3-level converters
Model Time Step = **580 ns**
17 kHz PWM

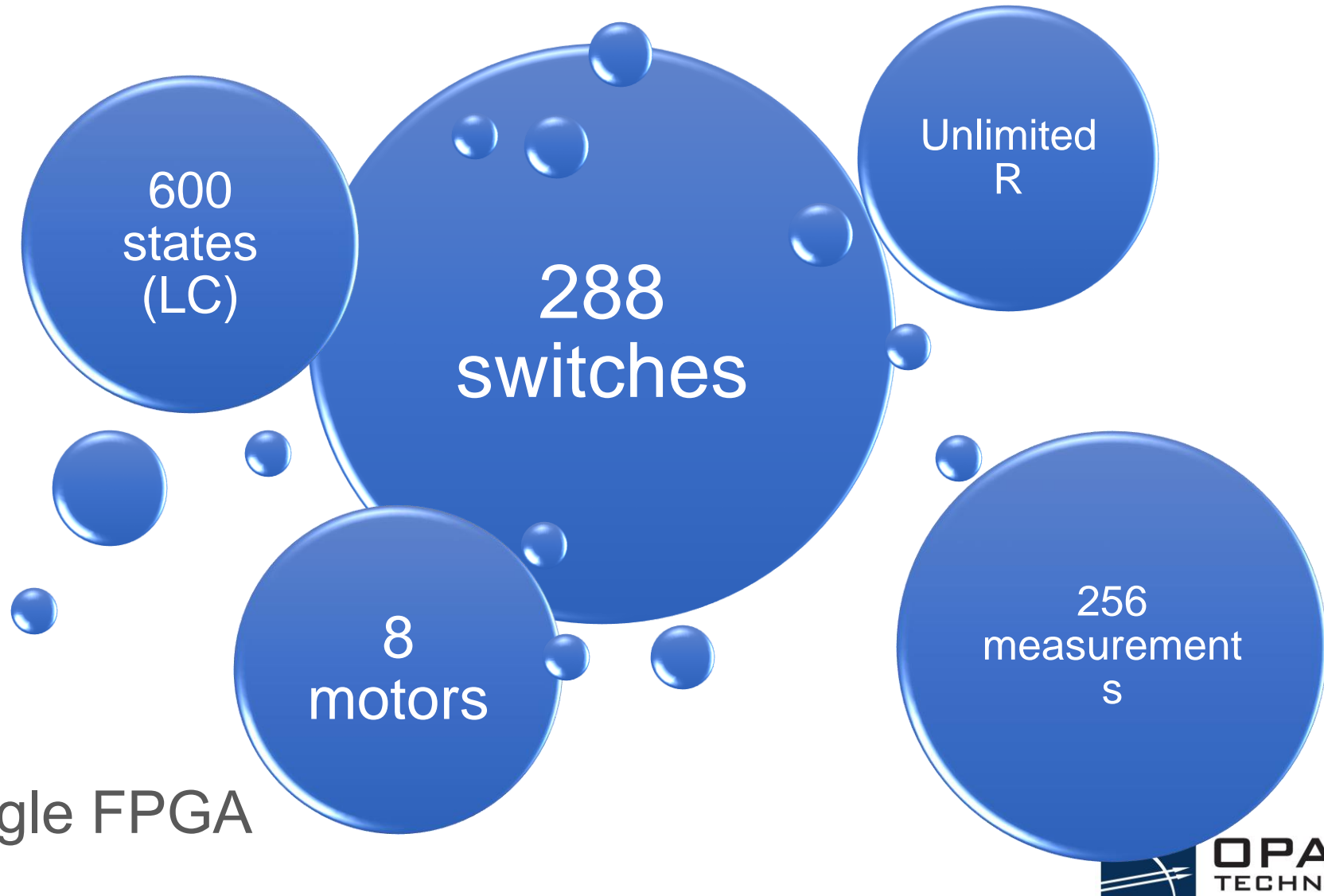
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MOTOR DRIVES – eHS CAPABILITIES

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NOW...



... On one single FPGA

APPLICATION CASES



DISTRIBUTION GRIDS

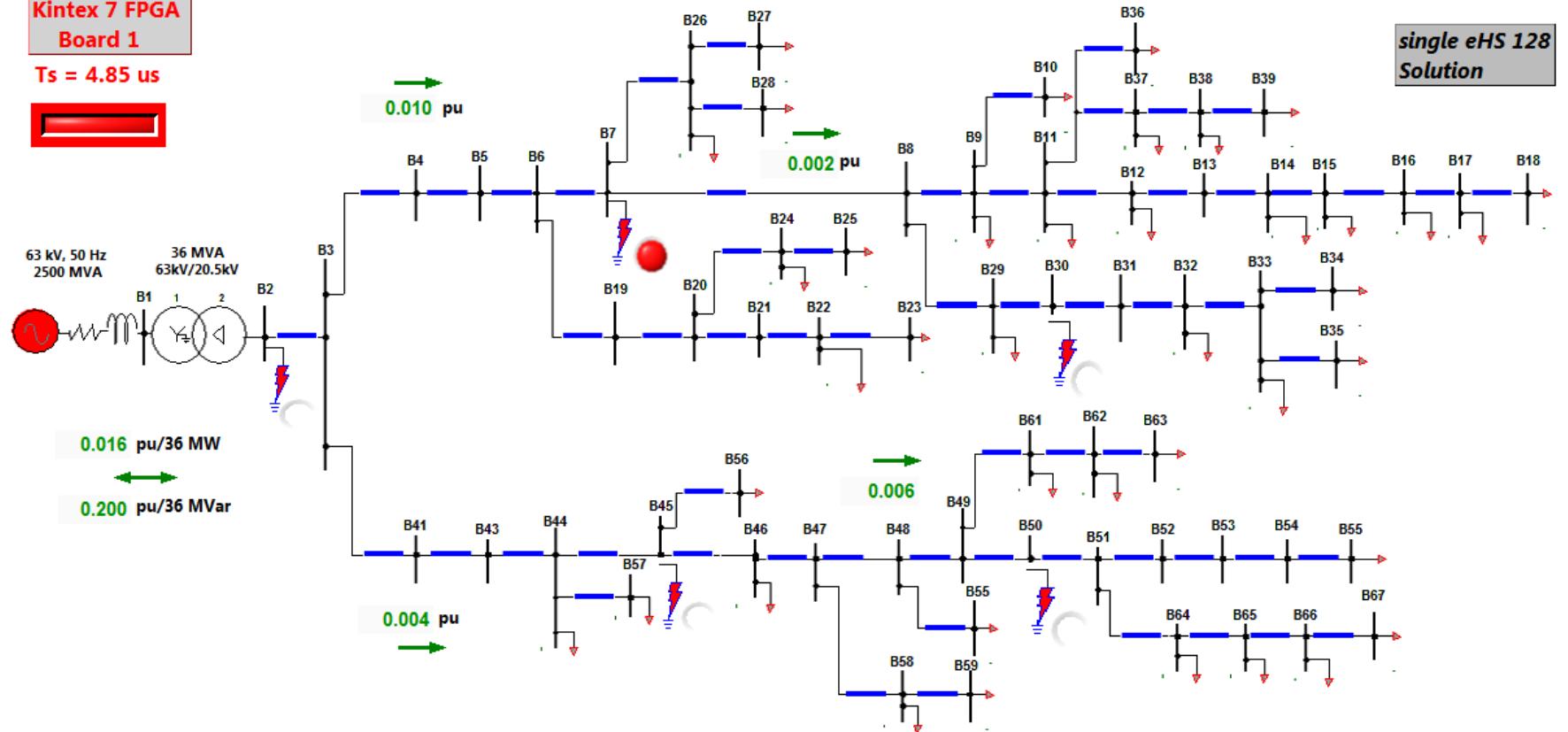
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1 FPGA

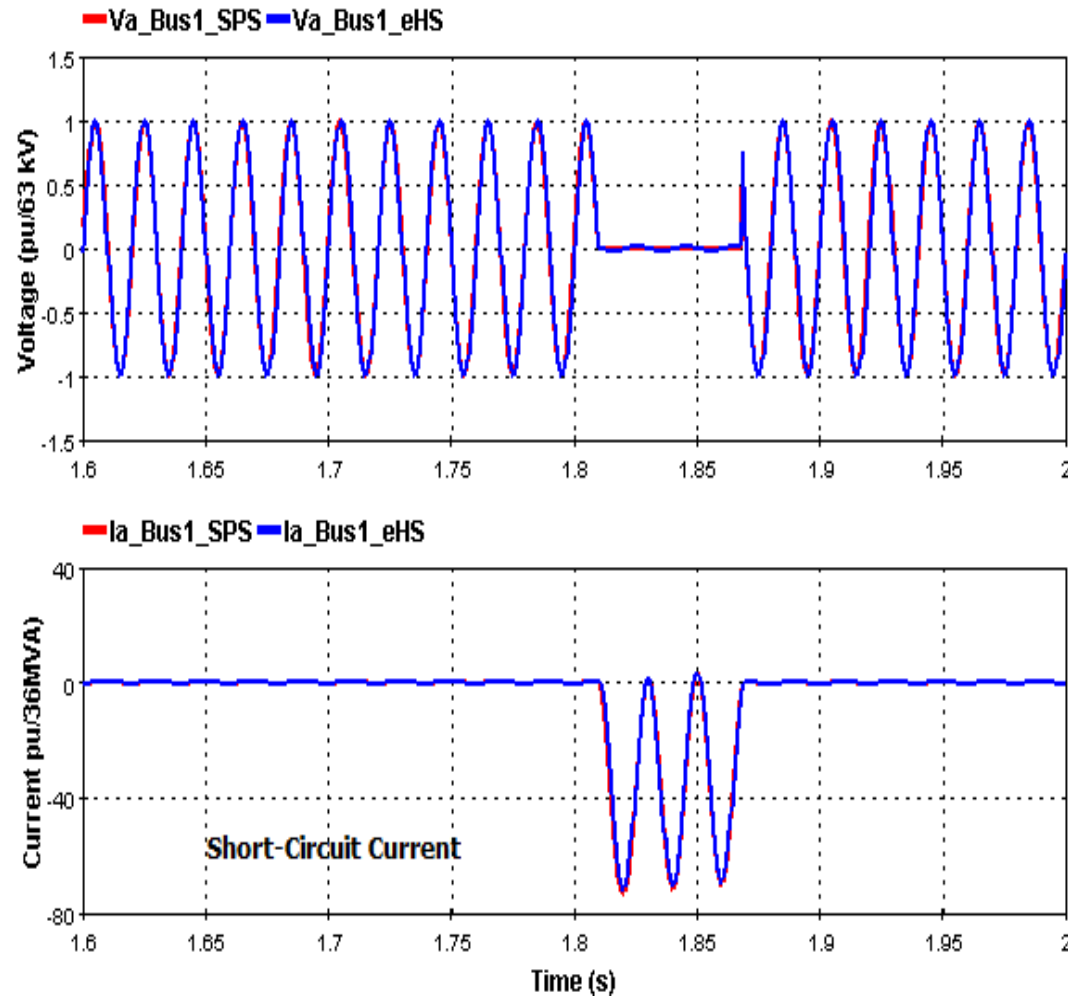
Kintex 7 FPGA
Board 1

$T_s = 4.85 \mu s$



-  : 62 3-Ph RL connections
-  : 41 3-Ph RL Loads
-  : 64 3-Ph Bus Bar
-  : 5 3-Ph Breaker Circuit

SPS offline vs eHS



DISTRIBUTION GRIDS



1 FPGA

Kintex 7 FPGA
Board 1





$T_s = 4.85 \mu s$

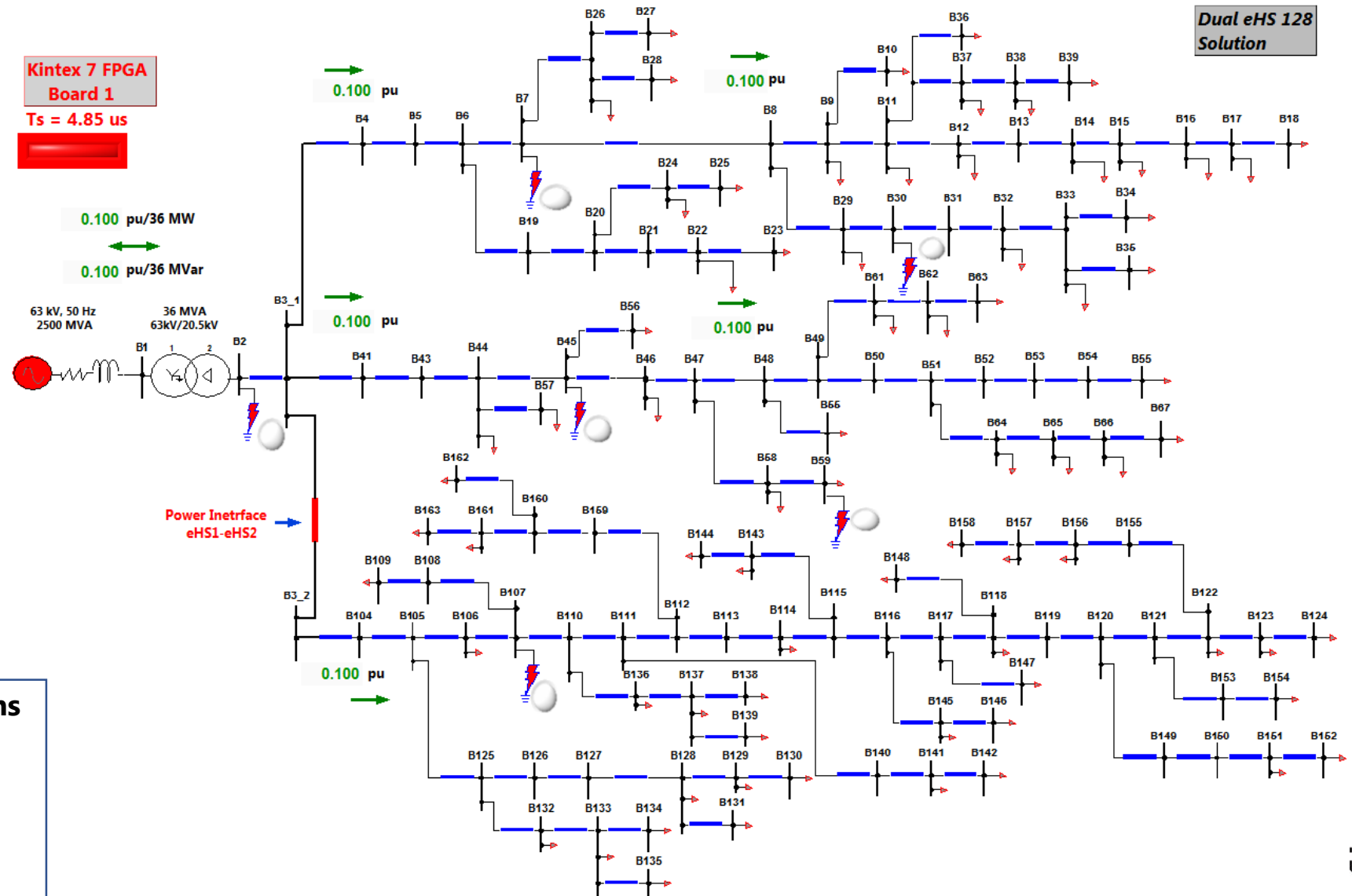
0.100 pu/36 MW

0.100 pu/36 MVar

63 kV, 50 Hz
2500 MVA

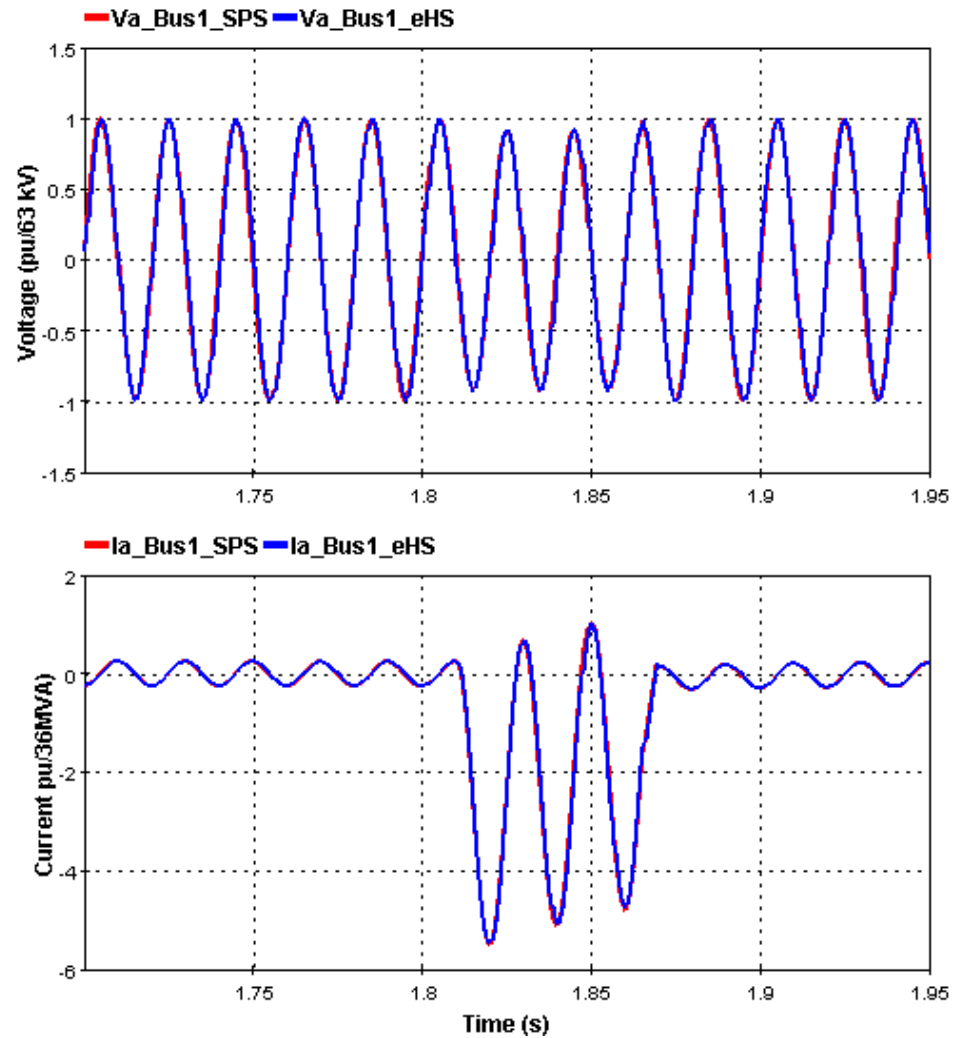
Power Inetrface
eHS1-eHS2

-  : 125 3-Ph RL connections
-  : 80 3-Ph RL Loads
-  : 129 3-Ph Bus Bar
-  : 5 3-Ph Breaker Circuit

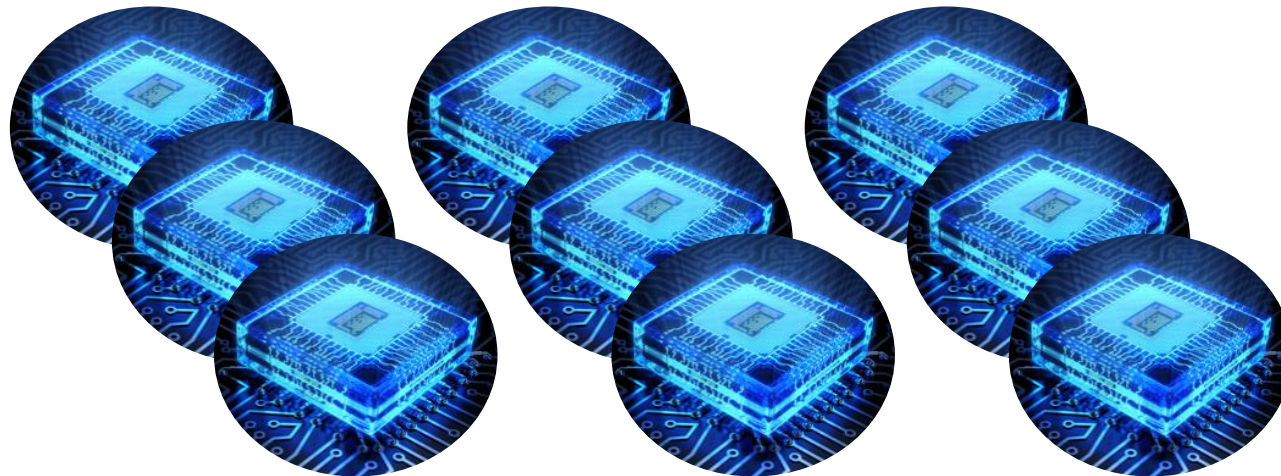


Dual eHS 128
Solution

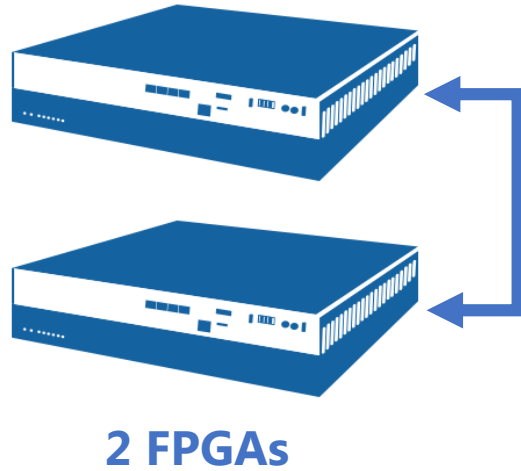
SPS offline vs eHS



- Reaching FPGA limits
- Future : **multi-FPGA** setups



DISTRIBUTION GRIDS



Kintex 7 FPGA
Board 1

$T_s = 2.5 \text{ us}$

63 kV, 50 Hz
2500 MVA

36 MVA
63kV/20.5kV

SFP Send/Receive

Power Inetrface
FPGA 1-FPGA 2

Kintex 7 FPGA
Board 2

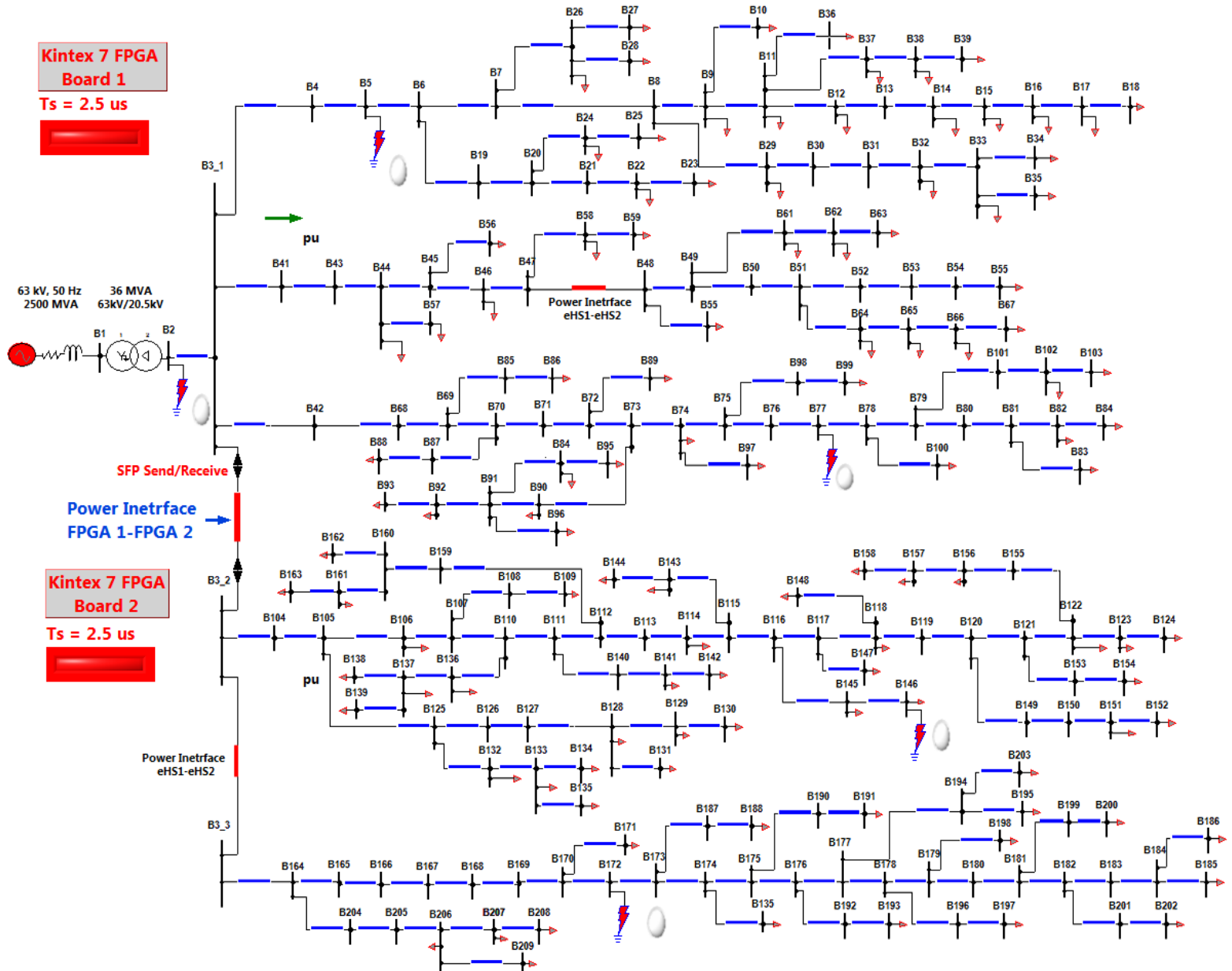
$T_s = 2.5 \text{ us}$

— : 208 3-Ph RL connections

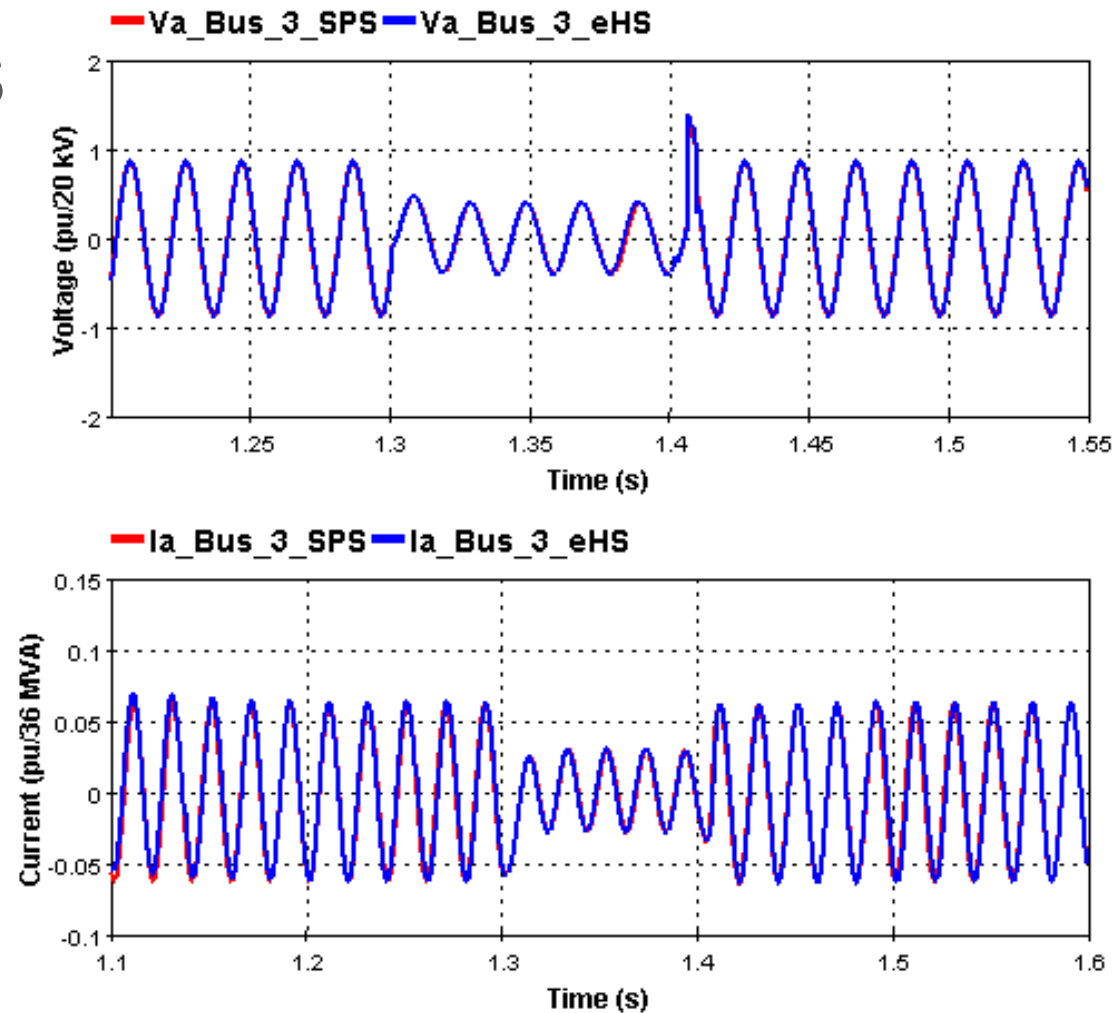
↓ : 124 3-Ph RL Loads

— : 210 3-Ph Bus Bars

⚡ : 5 3-Ph Breaker Circuit



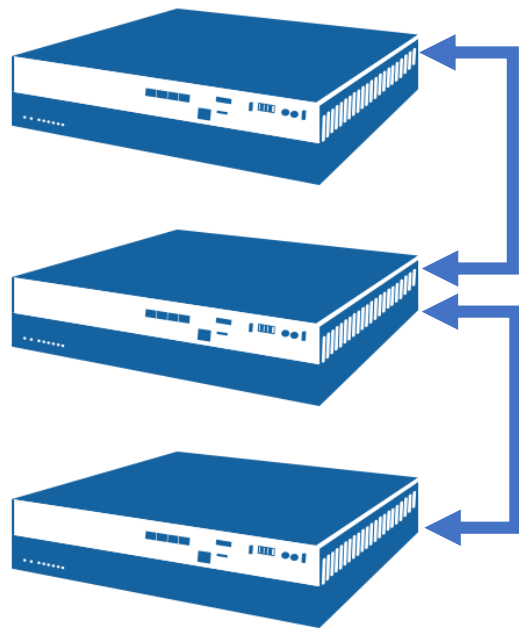
SPS offline vs eHS



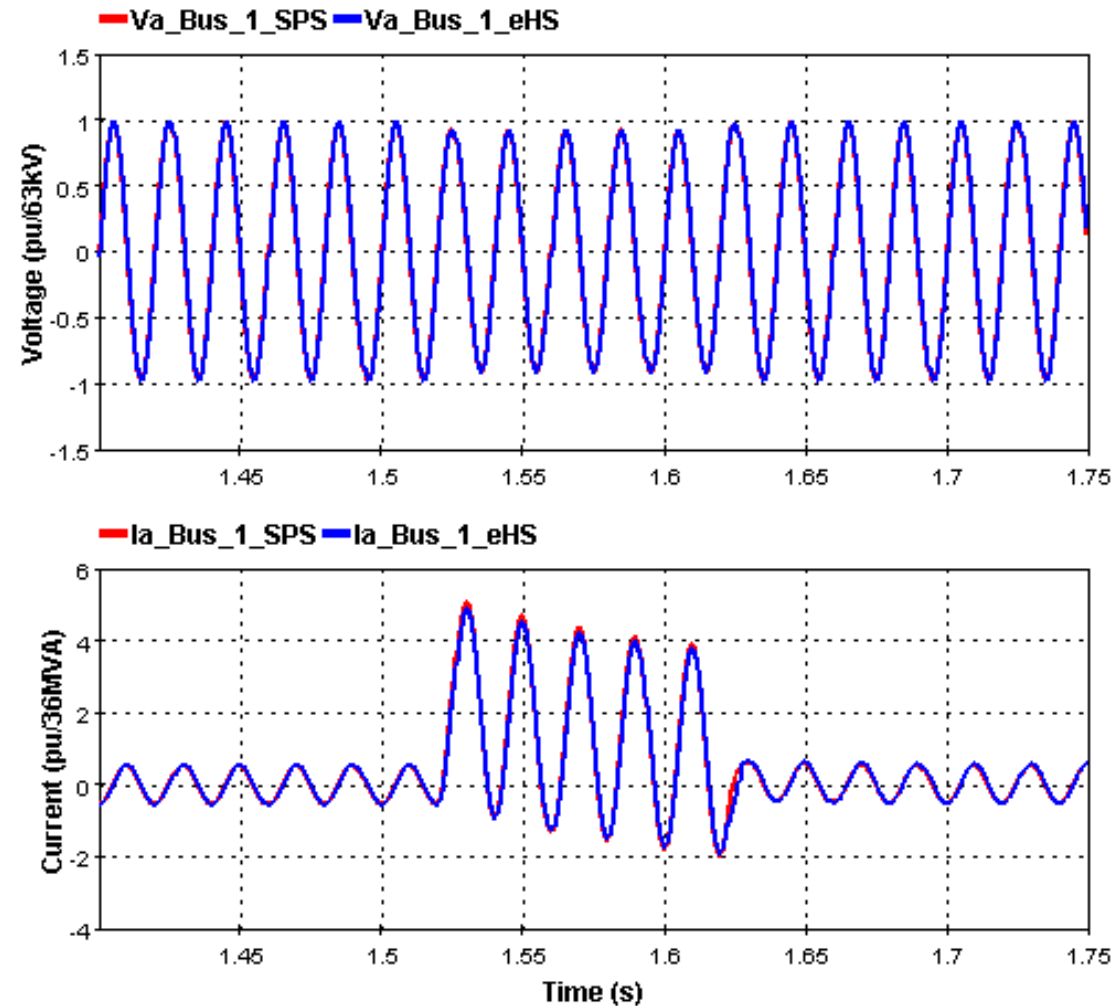
41



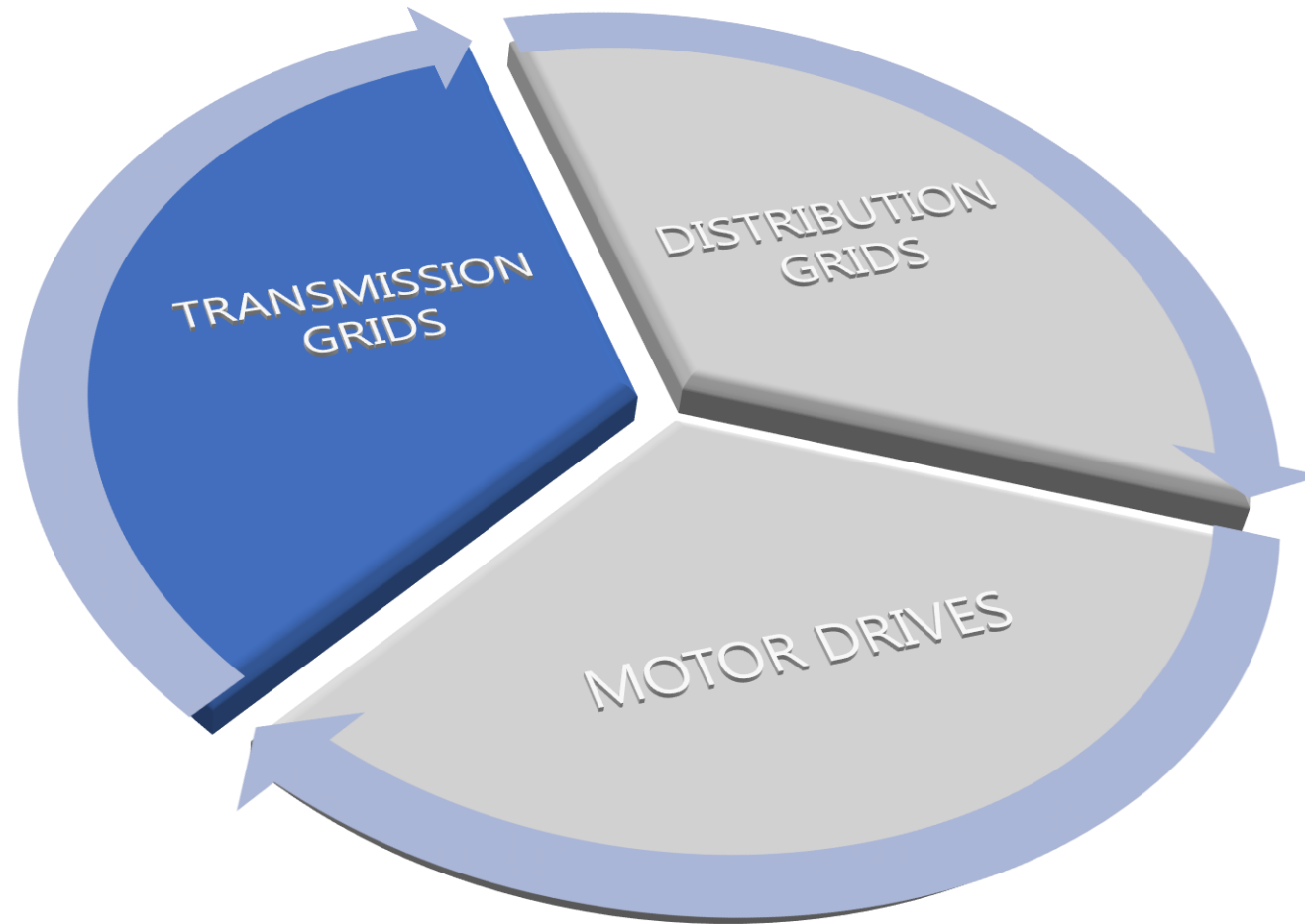
SPS offline vs eHS



3 FPGAs

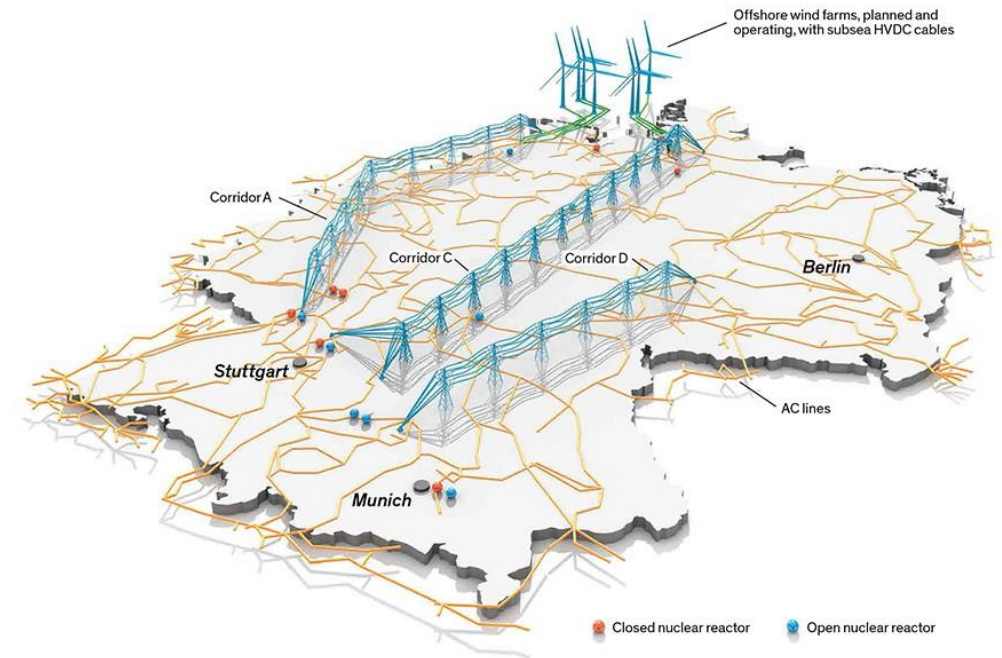


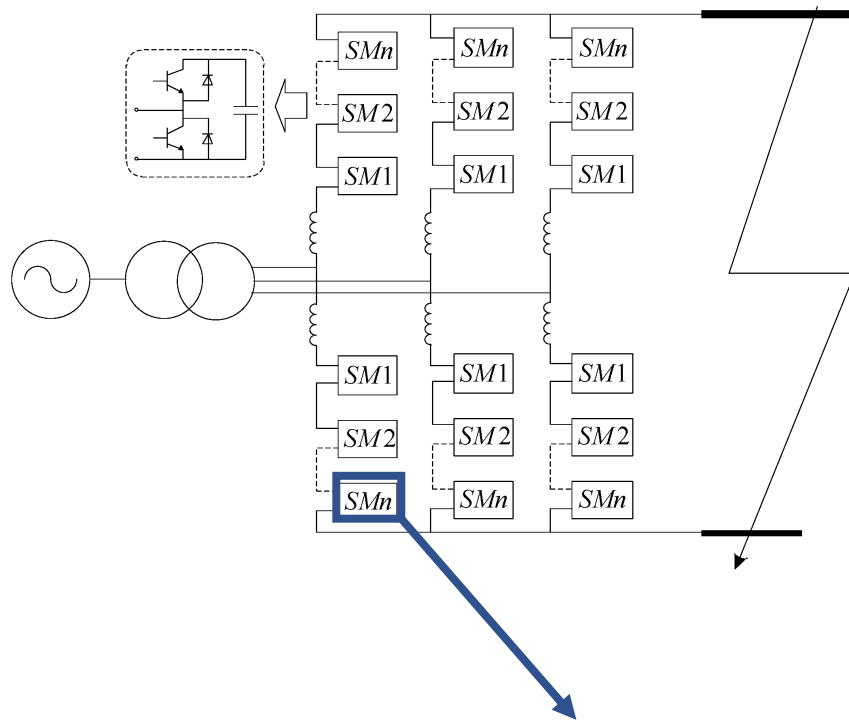
APPLICATION CASES



HVDC : High Voltage Direct Current

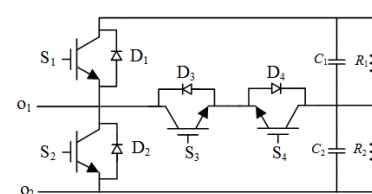
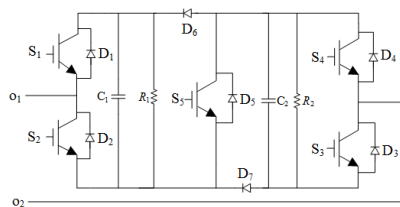
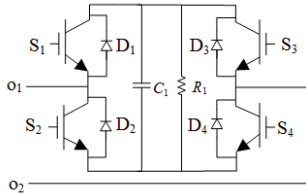
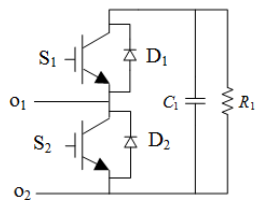
- Transmission lines
- Many advantages vs HVAC
 - Less electrical losses
 - Easy decoupling of AC grids
 - Better controllable
 - Cost affordable for longer distances
- MMC stations





MMC: Types of submodules

- Half-Bridge
- Full-Bridge
- Clamp-Double
- T-Type



Example of MMC-HVDC link **INELFE** (Spain-France)

- 401-levels
- 4800 half-bridge submodules
- 9600 IGBTs

How to simulate such a complex system
in **real-time**?



Source: www.siemens.com

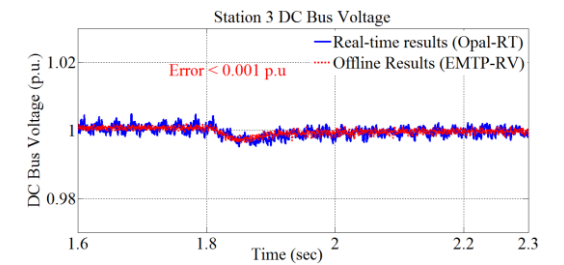
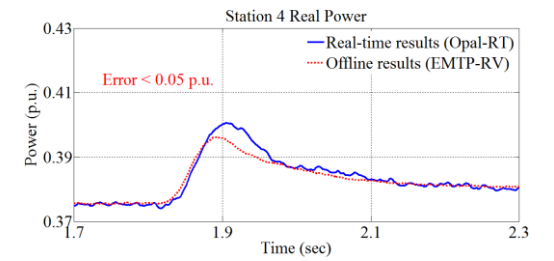
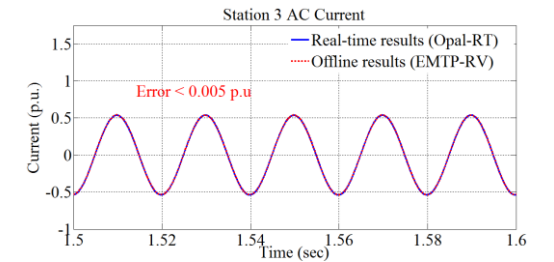
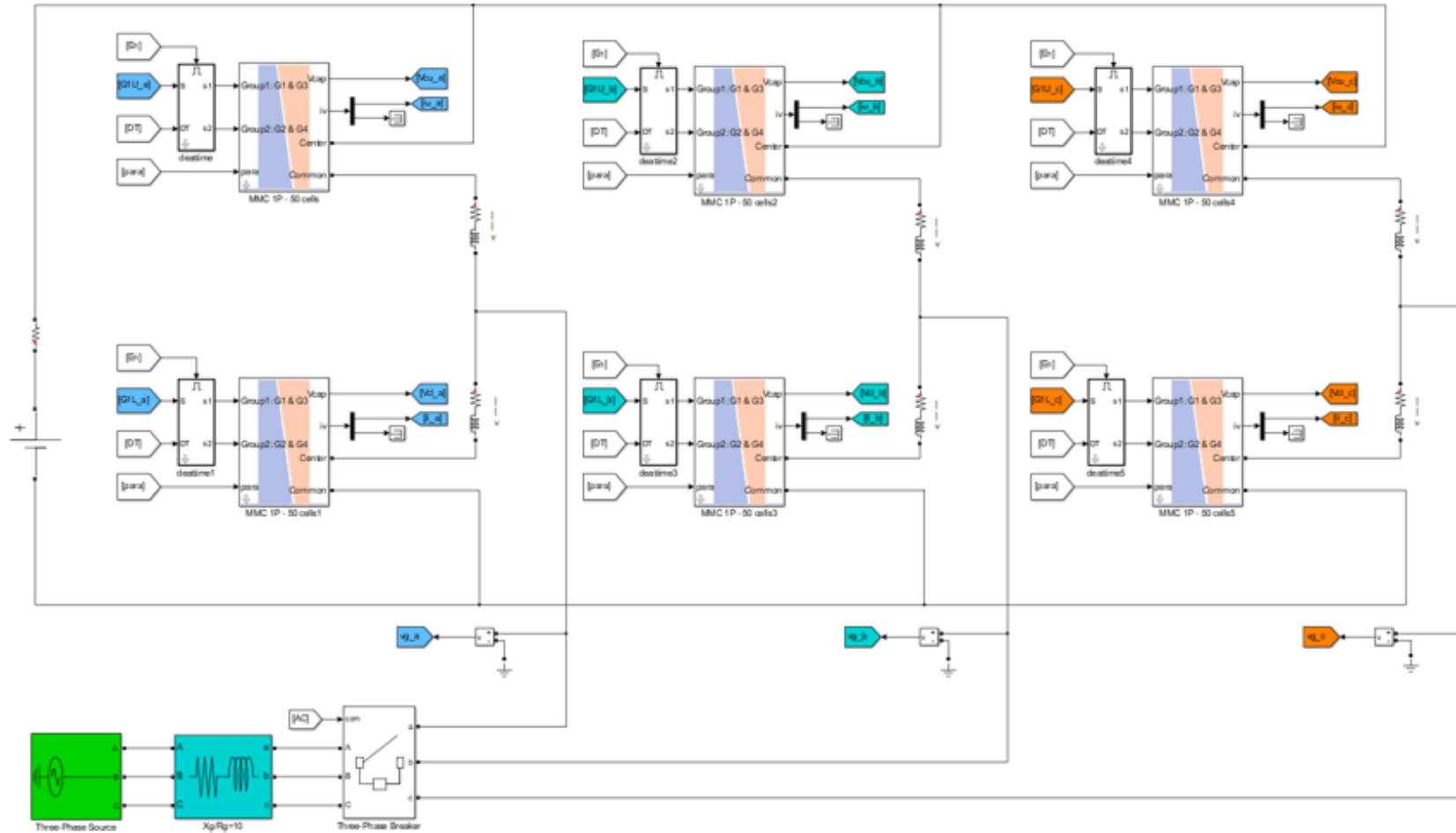
Challenges

- Complexity of converter
- Complexity of control
- Complexity of signal management
- Communication between control and converters/station

Solution

- FPGA Simulation of MMC
- Up to **6000 submodules** per FPGA
- **250 ns** time step
- Connection with controller : Aurora or Gigabit Ethernet
- Co-simulation with CPU which runs the station and grid models

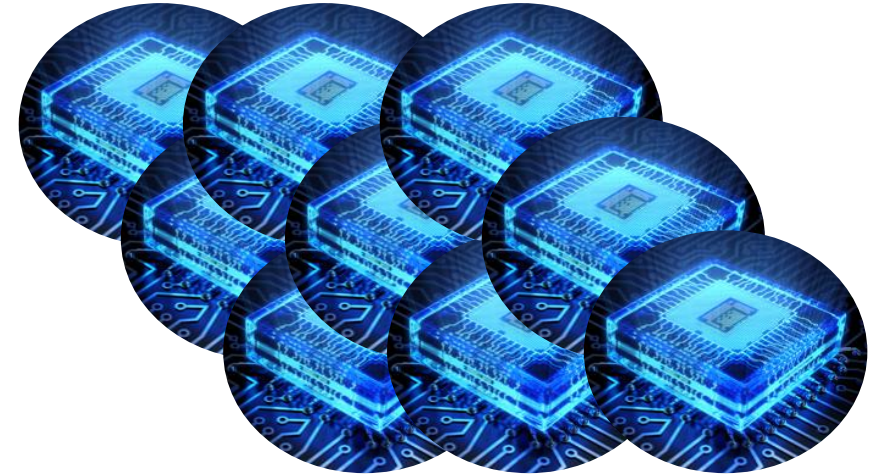
TRANSMISSION GRIDS



CONCLUSION



OPAL-RT





FROM
IMAGINATION...
TO REAL-TIME